mSI GMA: A Multilevel Full-Chip Routing System Considering SI Gnal-integrity and MANufacturability

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What is EDA?

Electronic Design Automation (EDA)

- Physical Design
  - Netlist → Layout (Geometry Representation)

Circuit design → Partitioning → Floorplanning & Placement → Routing → Compaction → Extraction & Verification → Fabrication
A Successful Story

Cadence confirms acquisition of Plato

Michael Santarini  Mike Santarini

EE Times
[03/14/2002 12:32 H EST]

SAN MATEO, Calif. — Countering threats to its bread-and-butter business in IC implementation tools, Cadence Design Systems confirmed Wednesday (March 13) that it has acquired IC routing start-up Plato Design Systems for an undisclosed amount.

The companies would not disclose the details of the acquisition. When EE Times broke the story Monday, sources said Cadence paid $60 million upfront and will pay to Plato an additional $25 million upon completion of certain goals. Cadence though said that number is incorrect, but would not say whether is higher or lower.

In the acquisition Cadence gains Plato's young but very promising NanoRoute...
**Agenda**

- Introduction
- Multilevel Routing Framework
- mSI GMA
- Conclusions

**mSI GMA:**
A Multilevel Full-Chip Routing Considering SI Gnal-integrity and MA nufacturability
Moore’s Law

- The number of transistors per chip **doubles** every 18 months.
- True in the past 40 years!
- Will be true in at least another 10 years, but now is facing lots of **red brick walls**.
Interconnect Problem

- Geometry of device and interconnect
  - Intrinsic delay of device
  - Local interconnect delay
  - Global interconnect delay


Source: Tutorial of ICCAD ‘00
Interconnect Problem

- Geometry of device and interconnect
  - Intrinsic delay of device
  - Local interconnect delay
  - Global interconnect delay


For 90 nm technology, interconnect delay will account for **75%** of the overall delay.

Source: Cadence Design System
Routing Problem

**Input:**
- Placement information (block location & pin location).
- Netlist.
- Timing budget for critical nets.
- Process parameters (R, C, \( \lambda \), etc.).

**Output:**
- Actual geometry layout for each net that meets design rules.
Routing Anatomy

Top View

3D View

Symbolic Layout

Pitch ($\lambda$)

Track

Via

Metal layer 2

Metal layer 1
As technology advances into nanometer territory, the paradigm shift of the routing problem is indispensable to cope with three major challenges:
- Design complexity problem
- Signal-integrity problem
- Manufacturability problem

A multilevel full-chip router considering signal-integrity and manufacturability (mSI GMA) is proposed to handle these challenges.
mSIGMA: A Multilevel Full-Chip Routing Considering Signal-integrity and Manufacturability
Routing Trends

- Billions of transistors may be fabricated in a single chip for nanometer technology.
- Need tools for very large-scale designs.
- Framework evolution for CAD tools:

Source: Intel at ISSCC-03
Two-Stage Routing

- **Global routing**
  - Partition the routing area into tiles.
  - Find tile-to-tile paths for all nets.
  - Attempt to optimize given objectives.

- **Detailed routing**
  - Assign actual tracks and vias for nets.
Flat Routing Framework

- Flat Framework
  - Sequential approaches
    - Maze searching
    - Line searching
  - Concurrent approaches
    - Network-flow based algorithms
    - Linear assignment formulation
  - Drawback: hard to handle larger problems
Hierarchical Routing Framework

- Hierarchical Framework
  - Top-down: divide and conquer
  - Drawback: lack the global information for the interaction among subregions
Multilevel Framework

- It has been successfully applied to partitioning, floorplanning, placement and routing in VLSI physical design and many more.

- Ingredients:
  - **Bottom-up Coarsening**: Iteratively groups a set of circuit components and collects global information.
  - **Top-down Uncoarsening**: Iteratively ungroups clustered components and refines the solution.
First Multilevel Global Router

  - Coarsening: Routing resource estimation
  - Initial global routing: Multicommodity flow algorithm
  - Uncoarsening: Constrained maze global routing algorithm

Coarsening

Level 0

Level k

Uncoarsening
Lin and Chang, ICCAD 2002.

- This framework integrates global routing, detailed routing, and resource estimation together at each level.
Track Assignment

- Traditional two-stage routing approach

A desirable intermediate step between *global* and *detailed routing*
An intermediate step (layer/track assignment) between coarsening and uncoarsening stage is introduced to do runtime and optimizations.

Perform congestion-driven pattern routing for local connections and then estimate routing congestion for the next level.

Perform layer/track assignment for long segments, and short segments are routed by a point-to-path maze router.

Use point-to-path maze routing to reroute failed net level by level.
## Multilevel Routing Framework Comparison

<table>
<thead>
<tr>
<th></th>
<th>Coarsening stage</th>
<th>Initial routing</th>
<th>Uncoarsening stage</th>
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<tr>
<td>Cong et al. in ICCAD 01</td>
<td>Resource estimation</td>
<td>Multicommodity flow</td>
<td>Global maze refinement</td>
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<td>Lin and Chang in ICCAD 02</td>
<td>Global routing</td>
<td>No initial routing</td>
<td>Global and detailed maze refinement</td>
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<td>Resource estimation</td>
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<td>Our Framework</td>
<td>Global routing</td>
<td>Track/layer assignment</td>
<td>Global and detailed maze refinement</td>
</tr>
<tr>
<td></td>
<td>Resource estimation</td>
<td></td>
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</tbody>
</table>

- **Our new framework**
  - *Fully utilizes the information of global router*
  - *Nets are routed in parallel*
  - *Suitable to address nanometer electrical effects*
mSIGMA: A Multilevel Full-Chip Routing Considering Signal-integrity and Manufacturability
Preprocessing

- Build routing tree for each net
- Decompose routing tree to two-pin nets
Tradeoff between MST and SPT

- **Minimum Spanning Tree (MST)**
  - Has the smallest total wire length
  - May incur longer path length

- **Shortest Path Tree (SPT)**
  - Has the shortest path length
  - May incur larger total wire length

Minimum Radius Minimum Cost Spanning Tree (MRMCST) is proposed for performance-driven routing tree construction.

*Radius*: length of $s$ to the farthest terminal
Union Graph of All MSTs

- Use **union** and **intersection graph** of all MSTs to preserve the minimum cost.
- Construct by modifying **Tarjan's edge coloring process**.

1) Sort edges by their length
2) Pick edges in increasing order

\[ O(n \lg n) \]

How to connect these blue components by choosing correct optional edges?
Locally Optimal Connection Strategy (LOCS)

Choose $e = (p, q)$ to minimize $F(e, T)$ where

$$F(e, T) = \text{dist}(c, p) + \text{cost}(e) + \text{dist}(q, pc(T)) + R_T$$

- $O(m_{opt} \log m_{opt})$

$m_{opt}$: number of optimal edges
Routing Model

- Partition a chip into tiles
- *Multilevel routing graph* \( G = (V, E) \)
  - Each node in \( V \) denotes a tile
  - Each edge in \( E \) denotes the boundary of adjacent tiles
Coarsening Stage

- Short nets are routed first for better routability
  
  \[ \text{R. Kastner et al., “Pattern routing: use and theory for increasing predictability and avoiding coupling,” TCAD, 2002.} \]
Pattern routing

- Uses L-shaped and Z-shaped connections to route nets.
- Has lower time complexity than maze routing.
Cost Function in Global Pattern Routing

\[ G_i = (V_i, E_i) : \text{multilevel routing graph at level } i. \]

Define \[ R_e = \{ e \in E_i \mid e \text{ is the edge chosen to route} \} \]

Then

\[
\text{cost}(R_e) = \sum_{e \in E} C_e,
\]

where \( C_e \) is the congestion of edge \( e \)

and

\[
C_e = \frac{1}{2(p_e - d_e)},
\]

where \( p_e \) and \( d_e \) are the capacity and density associated with \( e \), respectively.
Coupling Capacitance

• Deep submicron trends:
  • Interconnects dominate circuit performance
  • Wire heights scale at a slower rate than widths

Coupling can account for up to 70% of interconnect capacitance even in .25 micron designs.

*Sylvester et al., in Proc. VLSI Symposium on Technology, 1998.*
Crosstalk

- Coupling capacitance between segment \( i \) and \( j \).

\[ CC(i, j) = \alpha \cdot f_{ij} \cdot \frac{Len_{ij}}{Dist_{ij}^\beta} \]

- \( f_{ij} \): switching activities between \( i \) and \( j \).
- \( Len_{ij} \): coupling length.
- \( Dist_{ij} \): coupling distance.
- \( \alpha \) and \( \beta \): technology dependent constants.

- Crosstalk caused by coupling capacitance

**Aggressor Net**

**Victim Net**

**Functional Error**

**Timing Error**
Crosstalk Handling in Routing

Global routing → Information is not complete

\[ \frac{n}{m} : \text{congestion ratio} \]

Detailed routing → Not flexible

A Desirable Intermediate Step:

Layer/Track Assignment
Crosstalk-Driven Layer Assignment

Chip Layout

Interval Graph

Maximum spanning tree heuristic to extract edges with larger cost

Panel

Graph k-coloring heuristic on MST to separate edges to k layers
Crosstalk-Driven Track Assignment

Extract the maximum clique in the interval graph
Select the segment with maximum degree in the clique as the start point.
Crosstalk-Driven Track Assignment

Remove segments that can be allocated on track 1 but overlapped with segment b.
Crosstalk-Driven Track Assignment
Uncoarsening Stage

- Use point-to-path maze routing.
- Iterative refinement of a failed net is stopped when a route is found or several tries have been made.

Point-to-path maze routing

Coarsening stage

Uncoarsening stage
Our Multilevel Framework Recap

Perform congestion-driven pattern routing for local connection and then estimate routing congestion for the next level.

Use point-to-path maze routing to reroute failed net level by level.

Perform crosstalk-driven layer/track assignment for long segments, and short segments are routed by a point-to-path maze router.
Experimental Results

- **Language**: C++
- **Library**: STL, LEDA, LayoutDB (UCLA)
- **Platform**: 1GHz Sun Blade 2000 with 1GB memory
- **Benchmarks**:

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## Experimental Results

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<tr>
<th>Circuits</th>
<th>Results of Lin and Chang (ICCAD 2002)</th>
<th>Our Results</th>
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## Experimental Results

### Results of Lin and Chang (ICCAD 2002)

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<th>Circuits</th>
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<td><strong>1.3</strong></td>
<td><strong>1.2</strong></td>
</tr>
</tbody>
</table>

### Our Results

<table>
<thead>
<tr>
<th>Circuits</th>
<th>(D_{\text{max}})</th>
<th>(D_{\text{avg}})</th>
<th>(C_{\text{max}})</th>
<th>(C_{\text{avg}})</th>
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<td><strong>avg</strong></td>
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<td><strong>1</strong></td>
<td><strong>1</strong></td>
<td><strong>1</strong></td>
</tr>
</tbody>
</table>

- **\(D_{\text{max}}\):** Critical path delay (ps)
- **\(D_{\text{avg}}\):** Average net delay (ps)
- **\(C_{\text{max}}\):** Maximum coupling length (\(\mu\))
- **\(C_{\text{avg}}\):** Average coupling length (\(\mu\))

Crosstalk deterioration is not included in delay computation.

- **15\%** Reduced about
- **5\%** Reduced about
- **15\%** Reduced about
- **5\%** Reduced about
- **30\%** Reduced about
- **24\%** Reduced about
Experimental Results

Example of a routing result with GUI (s5378)
**Agenda**

1. Introduction
2. Multilevel Routing Framework
3. mSI GMA
4. Conclusions

**mSI GMA:**
A Multilevel Full-Chip Routing Considering Signal-integrity and Manufacturability
Solutions for Interconnect Problems

- Traditional timing optimization techniques:
  - Wire sizing
  - Buffer insertion
  - Gate sizing

- New IC technologies:
  - Copper and low-k dielectrics
  - X-architecture

The **X-architecture** is a new interconnect architecture based on the pervasive use of diagonal routing in chips, and it can shorten interconnect length and thus circuit delay.
Manhattan- vs. X-Architecture

Manhattan

X Architecture

Maximize Performance, same area

45°

X Smaller, Faster, Better Yielding Silicon

Source: Cadence
X-Architecture

- **X-initiative**
  - At least 42 members.
  - Veritable supply chain from IP and design implementation to photomask and manufacturing.

- Impacts on EDA tools:
  - Placement and **Routing**
  - Extraction
Perform trapezoid-shaped track assignment for long segments on trapezoid panels, and short segments are routed by a point-to-path maze router.

Perform congestion-driven pattern routing for local connections and then estimate routing congestion for the next level.

Use point-to-path maze routing to reroute failed nets level by level.

Perform trapezoid-shaped track assignment for long segments on trapezoid panels, and short segments are routed by a point-to-path maze router.
Benefits of Track Assignment

- Good for run-time reduction
- Effective for wirelength minimization

**Manhattan-Architecture**

- Wirelength: 5
- # Vias: 1 (VIA12)

**X-Architecture**

- Wirelength: $1 + 2\sqrt{2} \approx 3.828$
- # Vias: 3 (VIA12, VIA23, and VIA34)

Perform track assignment for longer and diagonal segments
Research on Octilinear Steiner Trees

- Related work:
  - C. S. Coulston, “Constructing exact octagonal Steiner minimal trees,” *GLSVLSI 2003*.

- For the previous approaches, those with relatively better quality may not achieve good efficiency.
Optimal 2-Terminal Net Routing Based on X-Architecture

- 2-terminal Net Routing
3-terminal Net Routing

Lemma:
The optimal routing solution of a 3-terminal net, of which one terminal is located in the merged region of the other two terminals, is the Octilinear Minimum Spanning Tree (OMST) of it.
Optimal 3-Terminal Net Routing: Case I

If the 3rd terminal is in region R4 (R4’)... The optimal 3-terminal net routing is the OMST of these three points.
If the 3\textsuperscript{rd} terminal is in region R2 (R2')…

The optimal 3-terminal net routing is the OMST of these three points and Steiner point a (b).
If the 3rd terminal is in region R1 (R1’, R3, or R3’)... The optimal 3-terminal net routing is the OMST of these three points and Steiner point S.
3-Terminal Net Routing on X-Architecture (X3TR)

Theorem:

The X3TR algorithm finds the optimal routing of the minimum wirelength for a 3-terminal net on the X-architecture in constant time.

Algorithm: X3TR (3-Terminal Net Routing on X-Architecture)

Input: A three-terminal net \( \Gamma = (\alpha, \beta, \gamma) \);

Output: The optimal routing tree \( T_o \).

begin
1 if (ThirdInsideMergedRegion(\( \Gamma \)) == True)
2 \( T_o = \text{OMST}(\Gamma) \);
3 else
4 \( \text{OutsidePT} = \text{FindOutsidePT}(\Gamma) \); 
5 if (OctalRegion(\( \text{OutsidePT} \)) == R4 || R4')
6 \( T_o = \text{OMST}(\Gamma) \);
7 else if (OctalRegion(\( \text{OutsidePT} \)) == R2 || R2')
8 \( \text{SteinerPT} = \text{ApexOfParallelogram}(\text{OutsidePT}) \); 
9 \( T_o = \text{OMST}(\Gamma, \text{SteinerPT}) \);
10 else if (OctalRegion(\( \text{OutsidePT} \)) == R1 || R1' || R3 || R3')
11 \( \text{SteinerPT} = \text{VerticalOfParallelogram}(\text{OutsidePT}) \); 
12 \( T_o = \text{OMST}(\Gamma, \text{SteinerPT}) \);
end
X-Steiner Tree Algorithm Based on Delaunay Triangulation

(a) Delaunay triangulation

(b) Compute optimal wirelength of OMST for each triangle and sort them

(c) Run X3TR for triangles in increasing order
Local Refinement for Wirelength

\[ 6 > 4\sqrt{2} \approx 5.6 \]
X-Steiner Tree Algorithm Based on Delaunay Triangulation

(a) Delaunay triangulation

(b) Compute optimal wirelength of OMST for each triangle and sort them

(c) $O(n \lg n)$
Multilevel X Routing Model

Partitioned Layout

Multilevel Routing Graph

tile

Metal 1
Metal 2
Metal 3
Metal 4
Global Pattern Routing: 1-Bend

1-Bend Pattern routing

(a) (b)
Global Pattern Routing: 2-Bend

2-Bend Pattern routing

Shortest path length: $\sqrt{2} \times \min(m, n) + |m - n|$
Trapezoid-Shaped Track Assignment Problem:

**Input:**
- A set of segments $S$
- A set of tracks $T$ in a trapezoid panel
- A cost function $F : S \times T \rightarrow N$, which represents the cost of assigning a segment to a track

**Objective:**
- Find an assignment that minimizes the sum of the costs.
Wire Pitch for X-Routing

Pitch for HV tracks

How to connect HV and diagonal tracks?

- Aligned track
- DRC-violated track
- Pessimistic track
- Virtual track

\[ \lambda \approx 7 (\lambda) \]

\[ 5 \times \sqrt{2} = 5 \times 1.414 \]

\[ \frac{\sqrt{2} \lambda}{2} < \lambda < \sqrt{2} \lambda \]
Connect to the Grid Point

Diamond-shaped global cell

Wrong-way jog

Detour!
Trapezoid Shape Track Assignment

- **Obstacles**
- **Left Segments**
- **Middle Segments**
- **Right Segments**

**Trapezoid Panel**
Perform trapezoid-shaped track assignment for long segments on trapezoid panels, and short segments are routed by a point-to-path maze router.

Coarsening

Uncoarsening

Perform congestion-driven pattern routing for local connections and then estimate routing congestion for the next level.

Use point-to-path maze routing to reroute failed nets level by level.

Perform trapezoid-shaped track assignment for long segments on trapezoid panels, and short segments are routed by a point-to-path maze router.
## Experimental Results

Compared with the Manhattan-based multilevel router, our X-router reduced wirelength by **18.7%**, average delay by **8.8%**, and run-time by **13%**.

<table>
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<tr>
<th>Circuits</th>
<th>Wirelength</th>
<th>#Vias</th>
<th>Cmp. Rates</th>
<th>D\textsubscript{avg}</th>
<th>Run-Time</th>
<th>Wirelength</th>
<th>#Vias</th>
<th>Cmp. Rates</th>
<th>D\textsubscript{avg}</th>
<th>Run-Time</th>
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<td>1.13</td>
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18.7% 8.8% 13.0%

ICCAD 2003:
T.-Y. Ho, Y.-W. Chang, S.-J. Chen, and D. T. Lee,
“A fast crosstalk- and performance-driven multilevel routing system.”

D\textsubscript{avg}: Average delay (Elmore delay model)
X Routing Results of S38417
mSIGMA: A Multilevel Full-Chip Routing Considering Signal-integrity and Manufacturability
Conclusions

- We have proposed a novel multilevel routing framework (mSIGMA) for nanometer challenges, such as:
  - Design complexity problem
  - Signal-integrity problem
  - Manufacturability problem

- Compared with the state-of-the-art multilevel router, the experimental results show that our mSIGMA achieves better routing quality of all aspects of these nanometer challenges.
Thank You for Your Attention!