Analog and Mixed-Signal Circuits
Testing and Design for Testability

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Outline

■ Overview of VLSI testing
■ Mixed-Signal Circuits Testing
■ Mixed-Signal Circuits Design-for-Testability
■ Summary
What is Testing?

- **VLSI realization process**

  1. Design House → IC Design
  2. Foundry → Wafer Manufacturing
  3. Foundry or Testing House → Wafer Testing
  4. Packaging House → Packaging
  5. Testing House → Final Testing

  ▶ Customer’s need (specifications) → Shipping

- **Testing**: The process of determining whether a system is functioning correctly or defective.
Why Testing?

- The IC fabrication process is not perfect!
  - Catastrophic defects
    - Underetched Via
    - Blocked Etch
  - Imperfect photographic printing & doping process
    - Focused ion beam (FIB) micrograph of metal traces on an IC
Why Study Testing? (1/2)

- **Economics!**
  - Reduce test cost (enhance profit)
    - 1 second of test time equals 3 to 5 cents.
    - 5 second test program @ 4 cents per second times one million devices per quarter costs USD 800,000 per year.
  - “Rule of Ten”:

<table>
<thead>
<tr>
<th>Defects detected during</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer</td>
<td>0.01 – 0.1</td>
</tr>
<tr>
<td>Packaged chip</td>
<td>0.1 – 1</td>
</tr>
<tr>
<td>Board</td>
<td>1 – 10</td>
</tr>
<tr>
<td>System</td>
<td>10 – 100</td>
</tr>
<tr>
<td>Field</td>
<td>100 – 1000</td>
</tr>
</tbody>
</table>
Economics!

- Shorten time-to-market (time-to-volume)
  - Profits depends on having product available at the right time.
  - Testing provides the means of maximizing product yields in the shortest possible time.
The quality of the tested circuit will depend upon the thoroughness of the test vector.

Exhaustive testing for a 3-input AND gate takes 8 test patterns.
Why Testing is Difficult?

- Consider a 32-bit adder
  - 65 inputs, 33 outputs:
  - $2^{65} = 36,893,488,147,419,103,232$ patterns
  - Using 10 GHz ATE, would take $\approx 116.98$ years

- Problems to think
  - A 32 bit adder (combinational)
  - A 64 bit counter (sequential)
  - A 1Gb memory
  - A $10^8$-transistor CPU
    - Combinational + sequential + memory
  - A mixed-signal processor
    - Combinational + sequential + memory + analog
So, Testing Cost Will Soon Be A Big Problem

- Testing cost vs. manufacturing cost

Source: ITRS Roadmap, 2002
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Analog/Mixed-Signal ICs

Transistors/Chip

Low  Medium  High

Volume

10^1  10^2  10^3  10^4  10^5  10^6

- Modems
- LAN Transceivers
- Consumer audio
- Video interfaces
- Codecs
- Servo
- ...

System-on-chip

Mixed signal ASIC

Dedicated interface components

MSI off-the-shelf components
Mixed-signal ICs surpassed the global microprocessor market last year (2005) [SIA]

The worldwide mixed-signal IC market is expected to reach $42.7 billion by 2007, representing a large 24% increase over the $34.4 billion mixed-signal IC market in 2004
Features of Mixed-Signal ICs Development

- Analog circuit contains fewer devices, whereas the digital part contains millions of devices
- High expenses both time and money on designing and testing of analog subcircuits
  - Absence of tools for analog and mixed-signal test development
Fact: Most of complicate digital ICs can be test in few seconds today.

- Structural based tests
  - Test faults rather than function
- There are fruitful research results to alleviate the difficulties
  - Fault simulation
  - Automatic test pattern generation (ATPG),
  - Design for Testability (DfT),
  - Built-In Self-Test (BIST),
  - ...
Analog Circuits Testing Difficulties

- Continuous time and amplitude signal
- Analog circuits are nonlinear in nature
- Complicated cause-effect relationship
- Absence of suitable fault model
  - Mainly functional (specifications) based test.
For complex MS ICs, testing is becoming one of the major cost factors in the overall IC product costs.

With the introduction of DfT techniques digital test costs came down.

Analog test costs will dominate the product costs.
A Beirf Summary of Mixed-Signal ICs Testing

- Expensive test equipment
- Long test time
- Long test developing time

To reduce test cost, the recently strategies are

- Reduce test items
- Employ low cost tester
- Computer aided test development
Various Circuit Types and Specifications (1/2)

- Analog and mixed-signal circuit types
  - Amplifier, comparator, filter, signal/reference generator, sensor/meter, transceiver (driver, transmitter, receiver, …), converter (ADC, DAC, VFC, …), …

- Analog and mixed-signal circuit specifications
  - DC specifications: gain, offset, drift, INL, DNL, …
  - AC specifications: unit-gain frequency, bandwidth, CMRR, …
  - Transient specifications: rise/fall/settling time, glitch, jitter, …
  - Others: operation range, I/O impedance, noise figure, power dissipation, temperature sensitivity, …
Various Circuit Types and Specifications (2/2)

Example: ADxxxx datasheet

- Analog front end for cable: 2x8bits ADCs, 1x10bits ADC, 1x12bits ADC, 1x12bits DAC (224 MHz, BW=65MHz)
- Datasheet gives 140 analog parameters
Reduce Test Items

- Characteristic observation inference test design approach [TCAD, 1999]
- Structural fault based specification reduction methodology [JETTA, 2002]
- Alternate test methodology [TCAD, 2002]

Specifications of initial N devices are measured using conventional test set-up.

Measurement data is taken for same set of N devices on alternate test set-up.

Model/Mapping Functions are built from measurements to specifications using statistical analysis.

Subsequent devices are measured on the alternate test set-up and models are used to estimate the specifications.
Test by Low Cost Tester

- One of the promising approaches to reduce test cost.
- In order to move to a low cost tester,

  Design for Testability (DfT) and/or Built-In Self-Test (BIST) techniques, and their corresponding control mechanism are necessary.
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Many DfT techniques largely reduce the test cost for digital circuits.

- Scan design, memory BIST, …
- Today, many CAD tools support DfT features.

Recently, many researchers toward to alleviate the difficulties of analog testing by using DfT techniques.

- Isolation (bypassing)
- Loop around
- SW-OPAMP
- Oscillation test strategy
Isolation (Bypassing)

- Normal
- Test functional block 1
- Test functional block 2

- Most used currently
- Switch (multiplexer) should be designed carefully
Example
  - CODEC, RF/IF Test

Switch (multiplexer) should be designed carefully

Fault masking
Switched-Opamp

- C = 1: regular opamp
- C = 0: power-off opamp
Test strategy

- C=1: normal operation test
- C=0: reconfiguration test

Example

\[ C_1 C_2 C_3 = 111 \]
\[ C_1 C_2 C_3 = 100 \]
\[ C_1 C_2 C_3 = 000 \]
Partitioning CUT into functional building blocks

Converting each building block to an oscillator

Defects cause deviations in oscillation frequency
Oscillation Test Strategy (2/2)

Example

- Continuous-time state-variable filter

Excellent for hard and large deviation faults

Challenges

- No universal rules to transfer DUT into oscillator
- No trivial relationship between the oscillation frequency and the specification under test
Practice

- Analog circuit designers design perfect circuits.
- No one dare to change it.

Sourced from: Prof. CC Su
So, What Should We Do …

- Incorporate DfT features at a early design stage
  - Analog design engineer(s) + test engineer(s)
  - Analog design engineer(s) who know(s) the knowledge of DfT issues
  - Develop easy-to-use test platform (including tools)
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AMS testing requires specialized approaches and experienced engineers because of the large varieties of signals, functions and circuits.

Mystification

- Testing is an expensive process that drives up the cost of ICs without adding any new value to the final product.
- Testing cannot change the quality of the individual ICs; It can only measure quality if it already exists.
  \[ \Rightarrow \text{Testing is not necessary!} \]

Demystification

- Guarantee IC quality and reliability
- Enhance IC yield
  - Infrastructure IP: design-for-yield
Thank You

Thank You for Your Patience!